R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

IN THE SPECIFICATION

The specification has been amended for consistency. Support for the amendments to the specification can be found in the drawings as originally filed, for example, on FIGS. 1-7 and in the specification as originally filed, for example, on pages 25, line 10 through page 30, line 4, on page 32, line 15 through page 33, line 11 and on page 48, lines 3-8. As such, no new matter has been introduced.

IN THE DRAWINGS

The objection to the drawings based on difficulty in reading the handwriting in the drawings (see page 2, section 1 of the Office Action) has been obviated by appropriate amendment and should be withdrawn. Labeling in the drawings has been repositioned and/or enlarged for legibility. The labeling has been amended for consistency with the specification. Specifically, the label on the output of block 196' in FIG. 5 has been changed from "Single_Error(8)" to "Single_Error(7)". Support for the amendments to the drawings can be found in the drawings as originally filed, for example, on FIGS. 1-7 and in the specification as originally

filed, for example, on pages 25, line 10 through page 30, line 4, on page 32, line 15 through page 33, line 11 and on page 48, lines 3-8. As such, no new matter has been introduced. Replacement drawing sheets are submitted herewith.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1-20 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-11 and 14-20 under 35 U.S.C. §103(a) as being unpatentable over Hsiao et al. (U.S. Patent No. 3,623,155, hereinafter Hsiao) in view of Horiguchi et al. (U.S. Patent No. 4,726,021, hereinafter Horiguchi) has been obviated by appropriate amendment and should be withdrawn.

Hsiao is directed to an optimum apparatus and method for check bit generation and error detection, location and correction (Title). Horiguchi is directed to a semiconductor memory having error correction means (Title). In contrast to Hsiao and Horiguchi, the presently claimed invention (claim 1) provides a bypass circuit configured to generate a second syndrome signal in response to the first syndrome signal and a bypass signal. Claims 14 and 15 include similar limitations. Neither Hsiao nor Horiguchi

teach or suggest a bypass circuit as presently claimed. Therefore, Hsiao and Horiguchi, either alone or in combination, do not teach or suggest each and every element of the presently pending claims 1, 14 and 15. As such, Claims 1, 14 and 15 are fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-13, 16-20 depend, either directly or indirectly from claim 1 or claim 15 which are believed to be allowable. As such, claims 2-13 and 16-20 are fully patentable over the cited references and the rejection should be withdrawn.

New claim 21 depends indirectly from claim 1 which is believed to be allowable. As such, claim 21 is fully patentable over the cited references.

New claims 22 and 23 include subject matter similar to original claim 11. Specifically, claim 22 provides a syndrome encoder circuit that comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate. Claim 23 depends directly from claim 22.

Contrary to the statement on page 12, lines 15-17 of the Office Action that "Hsiao and Horiguchi do not explicitly teach the specific use of specific circuitry for implementing the binary operations required by the syndrome generators taught in the Hsiao and Horiguchi patents," FIG. 3 of Hsiao shows that the check bit generator 2 and error detector 5 use **only** exclusive-OR gates (see FIG. 3 and column 10, lines 30-44 of Hsiao). Hsiao and Horiguchi are silent regarding a syndrome encoder comprising (i) non-inverting exclusive-OR gates **with an output inverted by a NOT gate**, (ii) **inverting exclusive-OR** gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) **non-inverting exclusive-NOR** gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) **inverting exclusive-NOR gates**, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate, as presently claimed. As such, claims 22 and 23 are believed to be fully patentable over the cited references.

Furthermore, despite the position taken on page 12, line 20 through page 13, line 16 of the Office Action, the Office Action fails to meet the Office's burden to present specific reasoning or factual findings to support the assertion of engineering design choice (see In re Chu, 36 USPQ2d 1089 (Fed. Cir. 1995). As such, claims 22 and 23 are fully patentable over the cited references.

The Office Action fails to provide sufficient reasoning to substantiate the position taken that the use of a particular set

of logic gates for the encoders and decoders of Hsiao and Horiguchi are obvious design choice. Specifically, the technical evidence provided in the specification militates against a conclusion that the implementation of the encoders and decoders of the present invention is merely a design choice. Furthermore, the Office Action's reliance on generalizations such as available circuitry, space requirements and operational speed requirements does not adequately address why the particular implementations claimed should be considered obvious. Furthermore, an inventor's explanation of how the invention works does not render obvious that which is otherwise unobvious. The Office Action has failed to present any prior art references that show the presently claimed embodiments. The teaching in the specification that the presently claimed embodiments provide space advantages and speed advantages is not evidence of obviousness. If anything, these teachings support the nonobviousness of the present invention that the use of the presently claimed embodiments reduces space requirements and speed. See *In re Glaug*, 283 F3d 1335, 62 USPQ 2d. 1151 (Fed. Cir. 2002).

Furthermore, the conclusory statements that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsiao and Horiguchi by use of specific circuitry for implementing the binary operations required by the syndrome generators taught be Hsiao and

Horiguchi" and "[t]his modification would have been obvious ... because one of ordinary skill in the art would have recognized that use of specific circuitry for implementing the binary operations required by the syndrome generators taught in the Hsiao and Horiguchi patents based on obvious engineering design choices such as available circuitry, space requirements and operational speed requirements and since that is what binary logic gates are for, to implement binary logic" do not adequately address the issue of motivation to modify. The factual question of motivation is material to patentability, and cannot be resolved on subjective belief and unknown authority (see In re Lee, 61 USPQ2d 1430 (Fed. Cir. 2002). It is improper, in determining whether a person of ordinary skill would have been led to a combination of references, simply to use that which the inventor taught against its teacher (see In re Lee at 1434 citing W.L. Gore v. Garlock, Inc., 220 USPQ 303 (Fed. Cir. 1983).

Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination (MPEP §2143.01). Since Hsiao describes the disclosed apparatus using **only** non-inverting exclusive-OR gates as optimum (see Title of Hsiao), Hsiao does not appear to provide a motivation or suggestion of the desirability of modifying the check bit generator/error detector circuit presented by the Hsiao reference

to obtain the invention as presently claimed. As such, the presently claimed invention is fully patentable over the cited references.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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